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13. ABSTRACT *(Maximum 200 words)*
This is the second annual progress report. The goal of this project is the improvement of epitaxially grown lattice-mismatched III-V compound semiconductors by development of a practical compliant substrate technology. During the past focused on a GaAs compliant substrate approach using material fabricated by epitaxial growth of an AlAs/GaAs structure with the subsequent oxidation of the AlAs. Although we observed changes in surface morphology and a small reduction in x-ray rocking curve linewidths of layers grown on these substrates, we were unable to confirm any significant defect reduction. During the latter part of the year we shifted our focus back to twist-bonded approach.

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Interfacial Bonding Research for Compliant Substrates

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Aims of the project

The goals of this research project as stated in the original proposal are "the improvement of epitaxially grown lattice-mismatched III-V compound semiconductors by development of a practical compliant substrate technology, and the use of this technology for the integration of optoelectronic emitters and detectors with silicon circuits." A key to our project is investigation of wafer-bonded compliant substrates for the subsequent growth of lattice-mismatched III-V compounds, including GaN. We will use our capabilities for epitaxial growth and *in situ* surface modification to prepare GaAs and Si wafer surfaces for direct wafer-to-wafer bonding. We will then bond those substrates in the same vacuum where their surfaces were prepared, assuring control over the surface composition and chemistry, and determine how the compliant substrates' properties depend on interfacial composition and bonding conditions.

During the past year, we focused primarily on compliant substrate fabricated by epitaxial growth of an AlAs/GaAs structure with the subsequent oxidation of the AlAs. The resulting polycrystalline aluminum oxide layer serves as the compliant support for a very thin (<20nm) GaAs substrate for the growth of InGaAs. More recently, we have shifted our focus back to a careful investigation of twist bonding and have begun to investigate the use of compliant support material comprising a semiconductor layer near its melting temperature.

Results

Oxidized AlAs approach

During the past year much of our activity on this program was focused on GaAs-Al_xO_y-GaAs structures to be used as complaint substrates for lattice-mismatched growth. Large-area substrates consisting of 16 nm of single-crystal GaAs over oxidized AlAs (i.e. Al_xO_y) were formed by lateral oxidation of patterned GaAs/$Al_{0.97}Ga_{0.03}$As/GaAs heterostructures. Wet digital etching (alternating oxidation and oxide removal) followed by dry iodine etching in the MBE growth chamber was used to prepare GaAs layers with thicknesses down to 16 nm. These layers were used as substrates for the growth of relaxed layers of $In_{0.15}Ga_{0.85}$As using either $In_{0.15}Ga_{0.85}$As or $In_{0.15}Al_{0.85}$As nucleation layers. The purpose of the experiments was to see if the 16 nm GaAs layers over oxidized AlAs would behave as compliant substrates and relax or partially relax the strain in InGaAs grown over them.

Epitaxial layers were successfully nucleated on these thin GaAs-on-oxidized AlAs layers. The $In_{0.15}Ga_{0.85}As$ epitaxial layers grown on these potentially-compliant substrates using an $In_{0.15}Al_{0.85}As$ nucleation layer showed none of the usual crosshatch pattern by Nomarski microscopy and had X-ray rocking curve line widths (FWHM XRD) that were narrower than those grown on bulk GaAs. FWHM XRD reduction corresponded to a calculated decrease of dislocation density by factor of 3. The growth of $In_{0.15}Ga_{0.85}As$ on the thin GaAs-on-oxidized AlAs layers without the $In_{0.15}Al_{0.85}As$ nucleation layer exhibited the usual crosshatch pattern and had no reduction in FWHM. Despite the smoother surface and FWHM XRD reduction which we observed in $In_{0.15}Ga_{0.85}As$, the layers are still not dislocation-free and we have seen no conclusive evidence of compliance in these substrates.

Wafer bonding approach

Our research focus has now shifted away from the oxidized AlAs compliant layer approach and toward two alternatives: a more careful study of the original "twist bonding" approach, and an approach using wafer bonding to introduce a semiconducting compliant layer near its melting point.

The papers on "twist bonding" which created much of the current interest in compliant substrate technology showed intriguing indications of compliance. Those studies have not been widely duplicated, and we believe that there have been no convincing demonstrations of significant threading dislocation reduction over large areas. Our current interest in this technique is to determine whether we can produce any observable reduction in threading dislocation count in InGaAs layers grown on thin (<200Å) GaAs layers created by twist bonding of two wafers followed by removal of one of the substrates. We have made observations which reinforce our conviction that the initial nucleation of the InGaAs layer is extremely important in determining the generation of dislocations in that strained epitaxial layer, and thus in determining whether the InGaAs layer can be grown dislocation-free and strained up to the critical thickness for the generation of dislocations in the compliant underlayer. Because we have made advances in preparation of wafer-bonded GaAs surfaces following removal of the top wafer and in wafer bonding, we are renewing our efforts on twist-bonded substrates.

We have recently begun a careful investigation of the surface roughness of GaAs and $In_{0.15}Ga_{0.85}As$ grown on thick (non-compliant) GaAs substrates, using atomic force microscopy. The purpose of the study of GaAs is to determine the suitability of these surfaces for wafer bonding. The mechanism of direct wafer bonding has been associated with the short range Van der Waals forces between atoms. In this case, the original wafer

surface micro-roughness becomes one of the most critical parameters. In references [1, 2] the surface criterion for direct wafer bonding process are theoretically and experimentally determined. It was shown that an RMS value of less than 5 Å is sufficient for the bonding process. We have grown two epitaxial structures consisting of a 100 nm $Al_{0.7}Ga_{0.3}As$ etch-stop layer followed by a 10 nm GaAs layer. The top surface (intended for bonding) was investigated by AFM. We found that the surface contains plateaus located on three levels with a difference of height of one monolayer. The surface grown on a SI GaAs (100) substrate has more extended plateaus than a surface grown on an n+ GaAs (100) substrate. However, the plateaus on each structure were sufficiently large that the RMS roughness was near zero for both cases. These surfaces appear to be very suitable for bonding, in agreement with our empirical observations in actually bonding such wafers.

We have characterized by AFM the surfaces of a series of $In_{0.15}Ga_{0.85}As$ layers grown on thick non-compliant GaAs(100). The purpose of this experiment is to establish the role of growth conditions on surface morphology for InGaAs grown on GaAs. Surface morphology may be measured quickly and easily with AFM. Deviations from planarity result from the strain in the growing layer, which is in turn related to the number and type of defects in the material. Therefore, differences in the surface morphology from sample to sample can quickly reveal qualitative information related to defects. Although we cannot unambiguously determine dislocation types and densities from surface morphology, we do expect that a reduction in threading dislocation density would result in an observable change in surface morphology. Thus, surface morphology becomes one means of making a rapid check for changes in defect density—i.e. we will look for differences in surface morphology between compliant and non-compliant substrates as one point of evidence for compliance.

In order to use surface morphology to look for changes in defect density due to growth on a compliant substrate, we have established a baseline growth process for InGaAs on thick GaAs substrates. We have used MBE to grow $In_{0.15}Ga_{0.85}As$ epilayers with thicknesses below (10nm) and above (100nm, 1000nm) the critical value for the formation of the dislocations. The substrate temperature was varied from 380°C to 510°C. We found that very different surface patterns are observed in layers with similar dislocation densities at the interface (assuming a similar degree of relaxation) which vary only in the growth temperature. The minimum roughness amplitude was obtained for samples grown at 450°C. We will compare these results with growth on compliant substrates.

We are also investigating another quick method of screening InGaAs defect density. We are using wet chemical etching and electrochemical etching to create etch pits in the surface of the material which decorate dislocations where they intersect the surface. This

process has been used for decades to count defects in bulk crystal boules, for example. Typically it is limited to relatively low defect densities, below about 10^6-10^7/cm^2, because long etching times are used to create large pits, observable with an optical microscope. With the advent of the AFM, much smaller structures are easily observed. There are literature reports of electrochemical etching being useful for detection at defect densities above 10^8/cm^2. We are developing etch chemistries and procedures to apply this technique to InGaAs epitaxial layers. This technique has applicability to the characterization of metamorphic epitaxy used for HEMT devices, and the development of this techniques is being done jointly with an industry-funded project on InP-based HEMT technology.

Another approach that will be used to evaluate the electrical quality of the compliant layers uses a near field scanning optical microscope (NSOM), which is being purchased using funds obtained through the 1999 Defense University Research Instrumentation Program (DURIP). We will use the NSOM to correlate topographical information with microscopic electrical characterization of threading dislocations by applying a near-field photovoltage technique developed by Hsu *et. al.*[3] Using this technique, we will evaluate the impact of surface undulations on the electrical properties (recombination lifetime) without the need for time consuming device fabrication and characterization. In addition to probing the epitaxial compliant layers, we will use this approach to investigate the quality of the bonded layer as well as lattice-mismatched interfaces and p-n junctions.

Plans for the coming year

For the coming year, we plan to proceed along three main directions. The first is to continue our careful examination of the existence of compliance in twist-bonded GaAs substrates. The AFM experiments described above set the baseline for comparison with non-compliant substrates. It is important to control the initial nucleation of the InGaAs layer to prevent the early formation of three-dimensional growth and the dislocations associated with island coalescence. We will investigate the use of migration enhanced epitaxy, low temperatures, and surfactants in this regard.

The second direction is to investigate the use of a nearly-melted compliant layer in a wafer-bonding approach. By bonding a wafer containing an etch stop and thin GaAs layer to a wafer topped with a thick relaxed InAsSb layer and then removing the top substrate, we can create a structure which comprises a very thin dislocation-free GaAs layer supported by the InAsSb layer. We can choose the InAsSb layer's melting temperature so that the growth of InGaAs over the thin GaAs layer occurs very near to that critical temperature. Motion of dislocations through the InAsSb should be very rapid near its melting temperature, facilitating compliance in that layer. We have tried this approach once

with an InSb layer obtained from researchers at Sandia. Unfortunately, the InSb melted at the growth temperature of InGaAs and the liquid surface tension caused the overlying thin GaAs to wrinkle and crack. Increasing the melting temperature by the addition of As should prevent this from happening.

Our third direction is to investigate the effect of etched mesa sidewalls on the reduction of dislocations. It has been reported in the literature that epitaxial growth on small mesas can induce migration of dislocations to the edge of the mesa. It is clearly necessary to have a material system in which lateral dislocation glide is enhanced for this approach to work over large areas. We will investigate this phenomenon in non-compliant and compliant substrate materials, including the nearly-melted antimonides. We will obtain the antimonide materials from other research groups.

Publications, Presentations, and Student Support

Publications and presentations during the past 12 months

1. "Lattice mismatched molecular beam epitaxy on compliant GaAs/Al_xO_y/GaAs substrates produced by lateral wet oxidation," D. Lubyshev, T. S. Mayer, W-Z. Cai, D. L. Miller, Proceedings of the Tenth International Conference on Molecular Beam Epitaxy, Aug.31-Sept. 4, 1998, Cannes, France, J. Crystal Growth **201/202**, 643-647 (1999).
2. "The effect of $Al_{0.7}Ga_{0.3}As$ etch stop removal on the preparation of wafer-bonded compliant substrates," C. Zhang, D. Lubyshev, T. N. Jackson, D. L. Miller, T. S. Mayer, J. Electrochemical Society **146** (4), 1597-1601 (1999).
3. "Fabrication of GaAs Based Compliant Substrates using Wafer Bonding and Lateral AlGaAs Oxidation," T. S. Mayer, D. Lubyshev, and D. L. Miller, *Advanced Heterostructure Workshop* , Kamuela, HI (1998)
4. "A comparison of wet and dry chemistries for hydrophobic silicon wafer bonding," J. B. Mattzela, P. A. Roman, J. Ruzyllo, and T. S. Mayer, to be presented at the 41st Electronic Materials Conference, Santa Barbara, CA (1999).

Students and others supported

Postdoctoral research scientist Dr. Dmitri Lubyshev, 50% FTE for the period 7/1/98-1/30/99.

Postdoctoral research scientist Dr. Nikolai Mochegov, 100% FTE for the period 3/15/99-6/31/99.

Graduate research assistant James Matzella, 25% FTE for the period 7/1/98-6/31/99.

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[1] "The effect of surface roughness on direct wafer bonding," C. Gui, M. Elwenspoek, N. Tas, J. G. E. Gardeniers, J. Appl. Physics, **85** (10), 7448-7454 (1999).

[2] *Semiconductor wafer bonding : science and technology*, Q.-Y. Tong, U. Gosele, John Wiley, New York, 1999.

[3] "Near-field scanning optical microscopy imaging of individual threading dislocations on relaxed Ge_xSi_{1-x} films," Hsu, J.W.P.; Fitzgerald, E.A.; Xie, Y.H.; Silverman, P.J., Appl. Phys. Let., **65** (3) 344-346 (1994).